What is claimed is :

1. A single ended three transistor quasi-static RAM cell comprising :
two cross coupled MOS transistors and one select MOS transistor connected to drain of one of the aforementioned MOS transistors wherein drains of both cross coupled MOS transistors are each connected to anode of one of two PN diodes functioning as loads .

2. The device of claim 1 further comprising a light source optically coupled to PN diodes , said PN diodes generating constant photocurrents due to large dynamic resistance .

3. The device of claim 2 wherein light is generated by large light emitting diode optically coupled to RAM memory chip containing aforementionrd RAM cells , said light emitting diode being operated in preferably constant or pulsed mode .

4. The device of claim 1 wherein reading is performed by precharging bit line of select transistor to low voltage and word line to voltage larger for at least value of aforementioned MOS transistor threshold voltage causing small positive or negative drain current of aforementioned select transistor without changing output voltage level of cross coupled transistors representing stored data , said stored data being represented during reading by direction of drain current , said drain current being detected by current or voltage sense amplifier .

5. The device of claim 1 being manufactured by standard CMOS technology , said device being physically diferent from standard CMOS memory cell by not having one select NMOS transistor and one PMOS load transistor .

6. The device of claim 1 wherein total capacitance connected to drain of cross coupled MOS transistor connected to select MOS transistor is larger than total capacitance connected to gate of the same cross coupled transistor .